Justin Liang

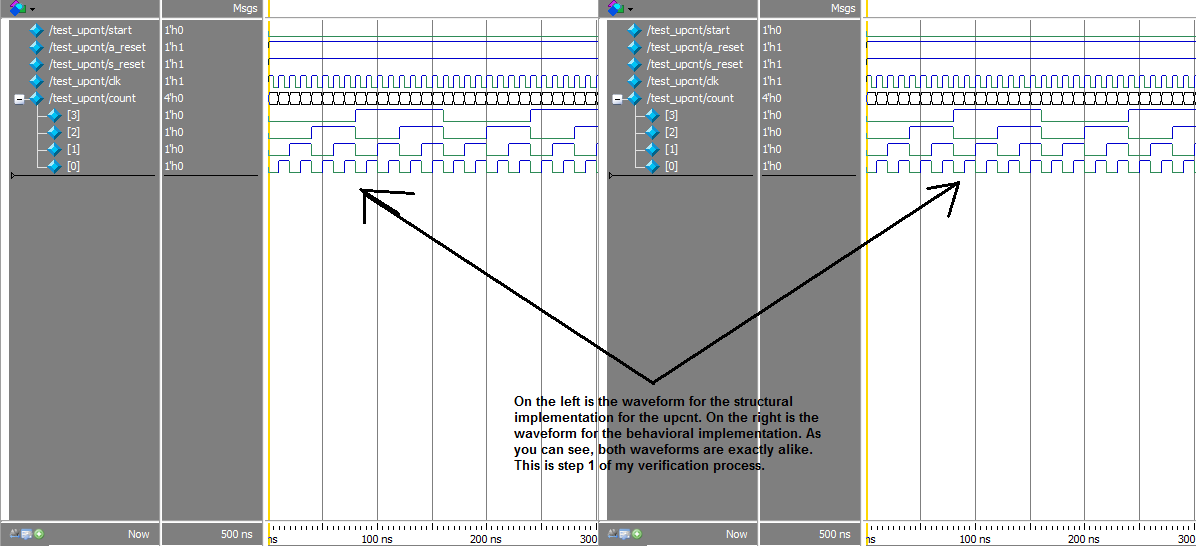
ECE 156A

Wang

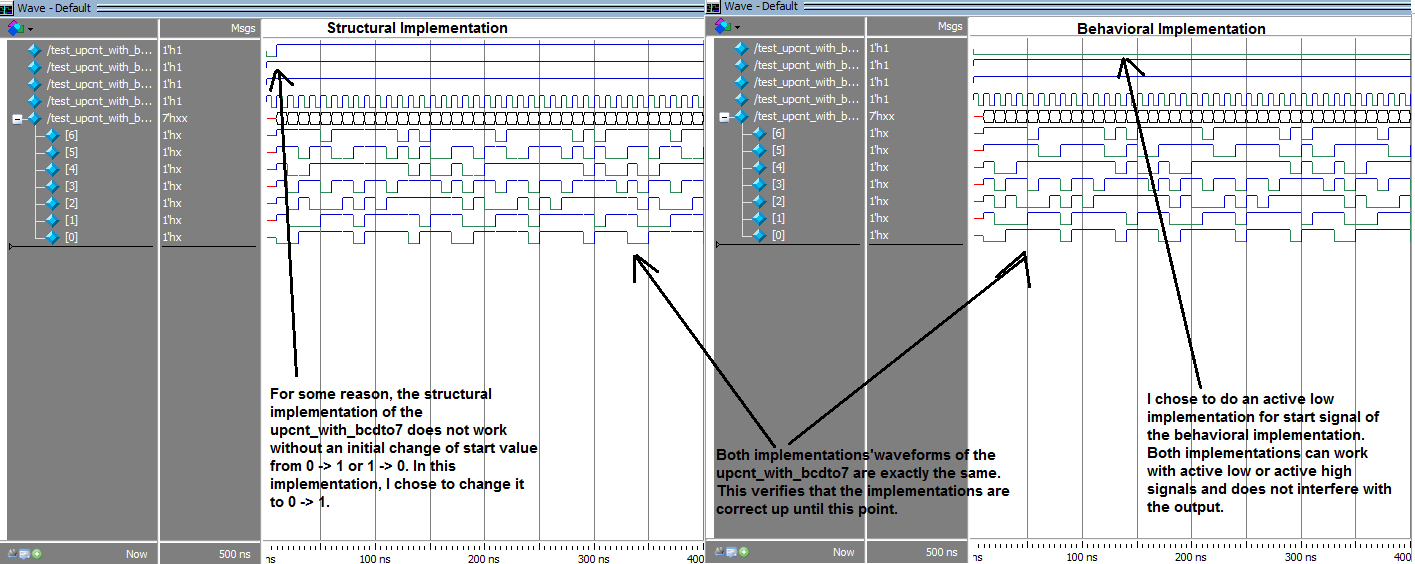
Homework #3

**Problem 1**

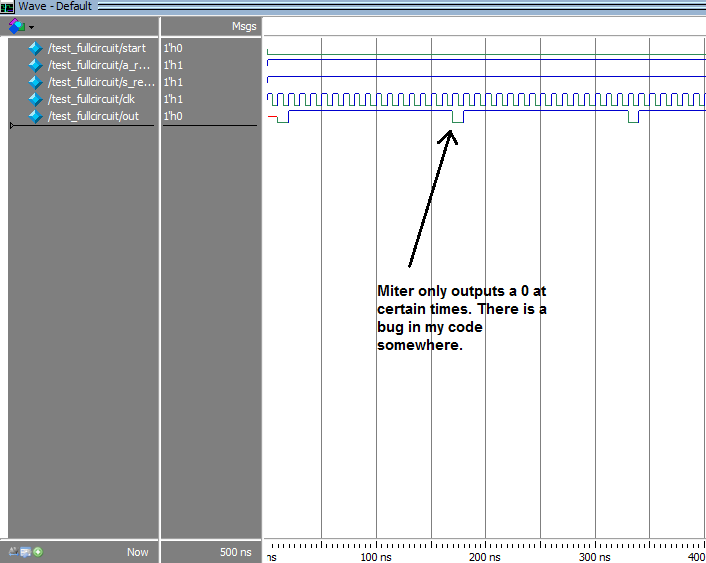
In this part of the homework, I ran into a bit of trouble getting the miter to work. In my attempt to solve the problem, I broke down the circuit into pieces. First, I created a test bench to test the structural implementation and behavioral implementation of the up counter. Below are the following waveforms:



As you can see, both waveforms are exactly alike, meaning that the up counter does not have problems when functioning by itself.

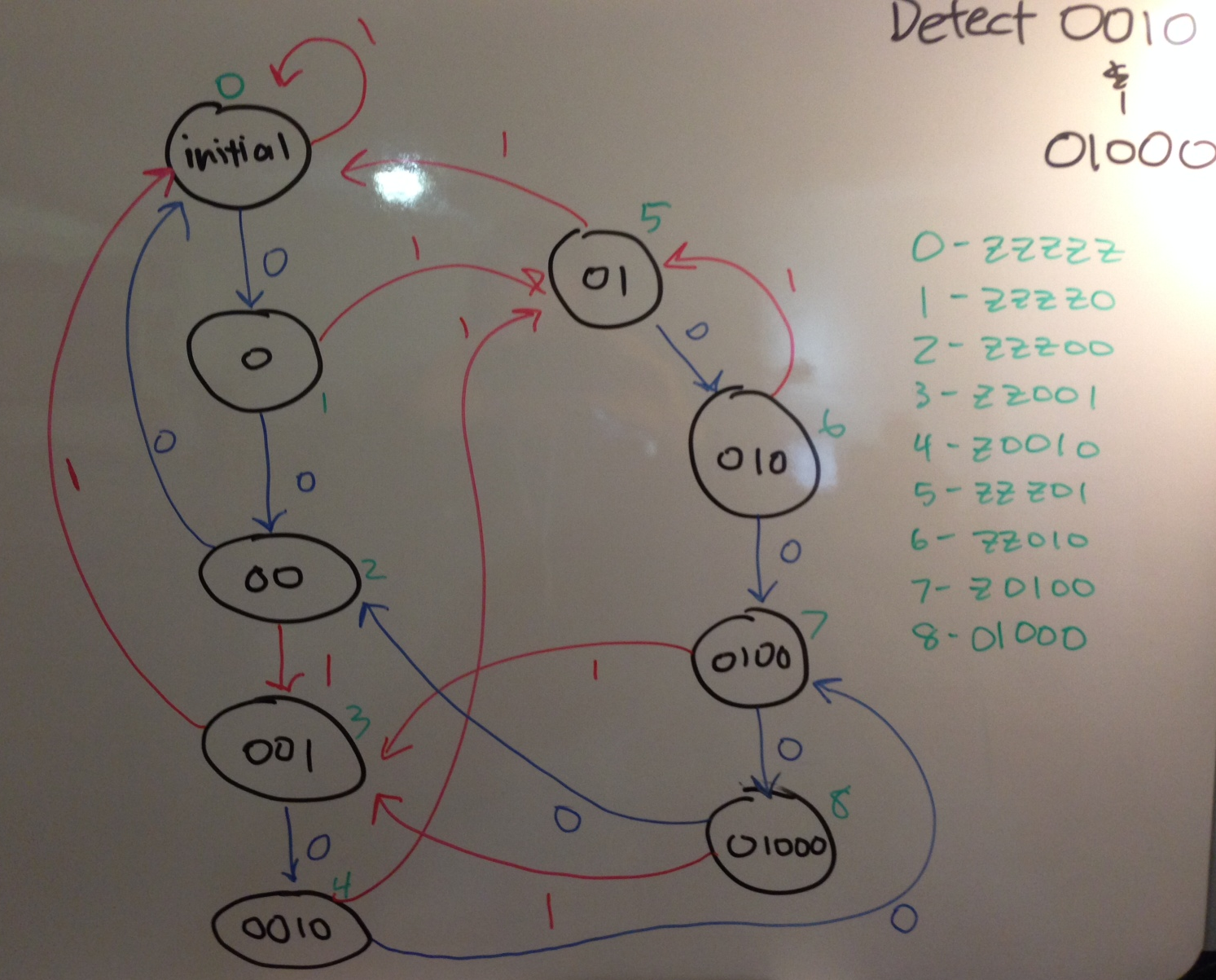
Secondly, I created a circuit that consisted of the up counter’s output driving the BCD to 7-segment decoder’s input. In my Verilog, this is called upcnt\_with\_bcdto7 and the corresponding testbench is test\_upcnt\_with\_bcdto7. Below is the following waveform.

As you can see, both implementations have the exact same waveform. This verifies that the problem is originating from either the miter, or the bug that causes the structural implementation not to work if I do not change the initial start value.

Lastly, when verifying both structural and behavioral implementations with the miter, I run into a problem where the miter outputs a 1 most of the time, and outputs a 0 sometimes. I have attempted to find the bug in my code, but the miter’s implementation is so simple that I think the problem is with my preceding circuit elements. Below is the following waveform of the full circuit which consists of the structural implementation of the up counter and BCD to 7-segment decoder, the behavioral implementation of the up counter and BCD to 7-segment decoder, and the miter.

Problem 2

In this part of the homework, I couldn’t get my code to produce the correct waveforms for both the behavioral and structural implementation. Below is the corresponding state diagram. I am pretty sure I did my state diagram correctly, but my code just isn’t working. Below is the corresponding state diagram. In this state diagram, I flipped the bits needed to be detected because inputs are read from right to left. 0100 becomes 0010 and 00010 becomes 01000.



Conclusion

Overall, the concepts for this lab were really easy as I have created an up counter, BCD to 7-segment display, and bit pattern detectors before. However, I just couldn’t get my code to work due to lack of time and minor bugs in the Verilog code. I am also not familiar with the concept of a miter, so maybe the problem in my code is my miter implementation. In my opinion, I think that the solutions for the previous homework should be released because each subsequent homework builds upon the previous homework. I have had trouble with my previous Verilog implementations, and now it is causing multiple bugs on the following homework.